REMARKS

Claims 1-7, 11-16 and 30-37 are pending. Claims 1-7 and 11-16 have been rejected. Claims 25-26 have been canceled. New claims 30-37 have been added. In view of the foregoing amendments and following remarks, the Applicants respectfully request allowance of the application.

Rejection of the Claims under 35 U.S.C. § 102

Claim 1 was rejected under 35 U.S.C. § 102(e) as being anticipated by DeKoning (U.S. Patent No. 6,148,368) (hereafter "DeKoning"). Applicant respectfully traverses this rejection.

To reject a claim under 35 U.S.C. § 102, the Office must demonstrate that each and every claim feature is identically described or contained in a single prior art reference. See *Scripps Clinic & Research Foundation v. Genentech, Inc.*, 18 U.S.P.Q.2d 1001, 1010 (Fed. Cir. 1991). As explained herein, it is respectfully submitted that the Office Action does not meet this standard, for example, as to all of the features of the claims.

Amended claim 1, for example, recites in relevant part: "an internal cache having a plurality of cache lines, each cache line sized to store a memory address and multiple data line lengths of data." DeKoning is directed to a RAID disk controller that uses segmented cache memory for accelerating disk array write operations. While DeKoning's cache memory 224 contains a plurality of cache segments (e.g., 225, 226), DeKoning's cache segments are merely segmented memory blocks. A segmented memory block is not a subdivided portion of a cache entry, instead, it is one or more cache entries allocated as a memory segment (e.g., memory block). There is no indication in DeKoning that each cache segment of DeKoning is ***one*** cache line ***sized*** to store a memory address and multiple data line lengths of data. Indeed, DeKoning

does not disclose any detail of the cache memory 224, which may be the conventional cache having deficiencies the presently claimed invention is designed to overcome. Therefore, DeKoning does not disclose each and every feature of claim 1. Withdrawal of the rejection is respectfully requested.

Rejection of the Claims under 35 U.S.C. § 103(a)

Claims 1-7 and 11-16 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Sachs et al. U.S. Patent No. 4,884,197 (hereafter "Sachs") in view of DeKoning. Applicants respectfully traverse the rejections.

The cited references Sachs and DeKoning fail to teach or suggest each and every feature of the independent claims 1 and 11. Even under KSR, obviousness is not shown unless the cited art in combination teaches all elements of the pending claims. *See*, *Ex Parte Wollenhaupt*, BPAI, Appeal No. 2007-3142 (Mar 13, 2008).

> Amended claim 1 recites a transaction queue that each queue entry comprises:
>
> a primary sub entry including an address portion and status portion, the status portion provided for a first external transaction corresponding to a first data portion of a respective cache line, and
>
> at least a secondary sub entry including a status portion provided for a second external transaction corresponding to a second data portion of the respective cache line, wherein the first and second data portions each stores a quantity of data corresponding to a data line.

Neither Sachs nor DeKoning teaches or suggests these features. Sachs is directed to a microprocessor architecture in which a cache memory is partitioned into an instruction section and a data section. The Office Action asserts Sachs's TLB 350 is equivalent to a transaction queue and refers to Sachs's ST, PL, SV, UV, D, R fields for storing status information of an external transaction. Office Action, pp. 7-8. However, Sachs's TLB 350 only provides "virtual

to real address translation" and Sachs's set of ST, PL, SV, UV, D, R fields collectively refers to one virtual address and consequently one external transaction. Sachs, col. 22, ll. 49-56. Although each TLB 350 entry has two halves: W and X subsystems, the W and X subsystems both have a virtual address, a real address and a set of ST, PL, SV, UV, D, R fields. There is no indication in Sachs of a primary sub entry with an address and status portion, and at least a secondary sub entry only having a status portion as claimed. Further, as described above, DeKoning refers to a RAID disk controller. DeKoning does not disclose anything related to a transaction queue. Thus, DeKoning does not cure the deficiencies of Sachs. Therefore, Sachs and DeKoning, either alone or in combination, fail to teach or suggest each and every feature of the independent claim 1. Withdrawal of the rejections of independent claim 1 and its dependent claims is respectfully requested.

Claim 11 has been amended to recite: "a transaction queue system comprising a plurality of queue entries, each queue entry to provide a sequence of external transactions, each ***external transaction of the sequence related to a single data line, the sequence of external transactions related to a single cache line***." Neither Sachs nor DeKoning teaches or suggests these features. As described above, Sachs's TLB 350 is for address translation. Although each Sachs's TLB 350 entry has two halves, there is no indication in Sachs that each TLB 350 entry provides a sequence of external transactions that ***each external transaction of the sequence related to a single data line***" and "***the sequence of external transactions related to a single cache line***" as claimed. Further, as described above, DeKoning does not cure the deficiencies of Sachs with respect to the transaction queue. Therefore, Sachs and DeKoning, either alone or in combination, fail to teach or suggest each and every feature of the independent claim 11.

Withdrawal of the rejections of independent claim 11 and its dependent claims is respectfully requested.

New independent claim 30 recites: "a primary sub entry including an address portion and status portion, the status portion provided for a first external transaction of the agent, and a secondary sub entry including a status portion provided for a second external transaction, ***the second external transaction addressing a second address adjacent to a first address stored in the address portion***." New independent claim 37 recites similar features. Neither Sachs nor DeKoning teaches or suggests these features. As described above, Sachs's TLB 350 is for address translation. A set of Sachs's ST, PL, SV, UV, D, R fields collectively refers to one virtual address and one external transaction. There is no indication in Sachs that each TLB 350 entry provides a first and second external transaction addressing adjacent memory addresses as claimed. Further, as described above, DeKoning does not cure the deficiencies of Sachs with respect to the transaction queue. Therefore, Sachs and DeKoning, either alone or in combination, fail to teach or suggest each and every feature of the new independent claims 30 and 37.

New dependent claims 31-36 depend from independent claims 1 and 30 respectively and are allowable at least for the same reason as their respective independent claims.

CONCLUSION

For all the above reasons, the Applicant respectfully submits that this application is in condition for allowance. A Notice of Allowance is earnestly solicited.

The Examiner is invited to contact the undersigned at (202) 220-4255 to discuss any matter concerning this application. The Office is hereby authorized to charge any additional fees or credit any overpayments under 37 C.F.R. § 1.16 or § 1.17 to Deposit Account No. 11-0600.

Respectfully submitted,
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